REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-4 and 11-22 are pending in this application. No claims are canceled, added, or amended by the present request for reconsideration.

In the outstanding Office Action, Claims 1-4 and 11-22 were rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent 5,117,380 to Tanagawa in view of U.S. Patent 6,698,662 to Feyt et al. (herein "Feyt"). Applicant respectfully traverses that rejection.

Claim 1 is directed to a data processing apparatus that includes an operation processing unit connected to a data bus and configured to perform a read cycle by outputting a read control signal to a memory, and perform a write cycle by outputting a write control signal to the memory. The data processing apparatus of Claim 1 also includes a pseudo-data generating circuit connected to the data bus, the read control signal output from the operation processing unit, and the write control signal output from the operation processing unit. The pseudo-data generating circuit is configured, in part, to generate pseudo-data and output the generated pseudo-data to the data bus according to an output timing based on the read control signal and the write control signal output from the operation processing unit. Independent Claim 11 includes similar features directed to a memory card.

Thus, in the apparatuses according to independent Claims 1 and 11, a pseudo-generating circuit is connected to the same data bus as the operation processing unit that performs memory read and write cycles. Further, based on the timing of memory read and write signals output from the operation processing unit, the pseudo-generating circuit may output pseudo-data to the data bus in between normal memory read and write cycles.

Applicant respectfully submits that Tanagawa and Feyt fail to teach or suggest each of the features of independent Claims 1 and 11. For example, Applicant respectfully submits

that Tanagawa and Feyt fail to teach or suggest generating pseudo-data and outputting the generated pseudo-data according to output timing based on a read control signal and a write control signal output form an operation processing unit. Further, Applicant respectfully traverses the assertion in the Office Action at page 3, lines 10-17, that Tanagawa discloses a pseudo-data generating circuit that outputs pseudo-data based on read and write control signals at Tanagawa Fig. 2 and column 3, lines 8-18.

Tanagawa describes a random number generator that is driven by clock pulses from a clock source independent of a system clock source.[1] According to Tanagawa, counters 5 and 6 receive clock pulses from an independent clock, and

> [w]hen a random number is required, the read signal is driven high for an interval T1 in FIG. 2. During this interval the inverse of the read signal is low, so the outputs of the AND gates 3 and 4 remain low and the counters 5 and 6 stop counting. In addition, the output enable (OE) inputs of the counters 5 and 6 are high, so the read-out control circuits 7 and 8 output the counter contents Q1 to Q16 to the system bus 9. Since the counters 5 and 6 operate independently of each other and of the system clock, the value output from Q1 to Q16 is in effect a random number.[2]

In other words, according to Tanagawa, a random number generator generates random numbers based on clock signals that operate independent of a system clock, and the random numbers are output to the data base based on a timing of only a read signal RD. However, it is respectfully submitted that Tanagawa is silent regarding any outputting of random numbers based on a timing of a write signal from an operation processing unit. Further, Applicants respectfully submit that Feyt also fails to teach or suggest that feature.

Thus, Applicant respectfully submits that Tanagawa fails to teach or suggest "a pseudo-data generating circuit connected to said data bus . . . configured to generate pseudo-data and output the generated pseudo-data to said data bus

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[1] Tanagawa at Abstract.
[2] Tanagawa at column 3, lines 8-18.

according to an output timing based on said read control signal and said write control signal output from said operation processing unit," as required by Claim 1 and as similarly required by Claim 11.

Therefore, Applicant respectfully submits that independent Claims 1 and 11 patentably define over Tanagawa and Feyt, whether taken individually or in combination.

Further, Applicant respectfully points out that the outstanding Office Action fails to assert any specific teachings of Tanagawa or Feyt with respect to the features recited in independent Claims 3 and 13.

On the other hand, Applicant respectfully submits that Tanagawa and Feyt also fail to teach or suggest each of the features of independent Claims 3 and 13. For example, for reasons similar to those noted above with respect to Claims 1 and 11, it is respectfully submitted that Tanagawa and Feyt fail to teach or suggest "a control signal generating circuit configured to receive said read signal and said write signal from the operation processing unit, detect a change in the read signal or a change in the write signal, and generate a control signal based on the detected change," as required by independent Claims 3 and 13. Further, for reasons similar to those noted above with respect to Claims 1 and 11, it is respectfully submitted that Tanagawa and Feyt also fail to teach or suggest "a pseudo-data generating circuit connected to said data bus and configured to receive the control signal from the control signal generating circuit, generate pseudo-data, and output the generated pseudo-data to said data bus in accordance with the control signal," as required by independent Claims 3 and 13.

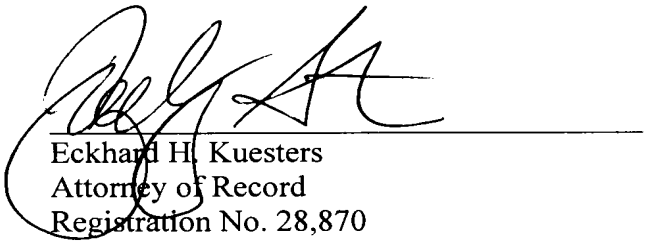
Thus, it is respectfully submitted that independent Claims 3 and 13 also patentably define over Tanagawa and Feyt, whether taken individually or in combination.

Accordingly, Applicant respectfully submits that independent Claims 1, 3, 11, and 13, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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